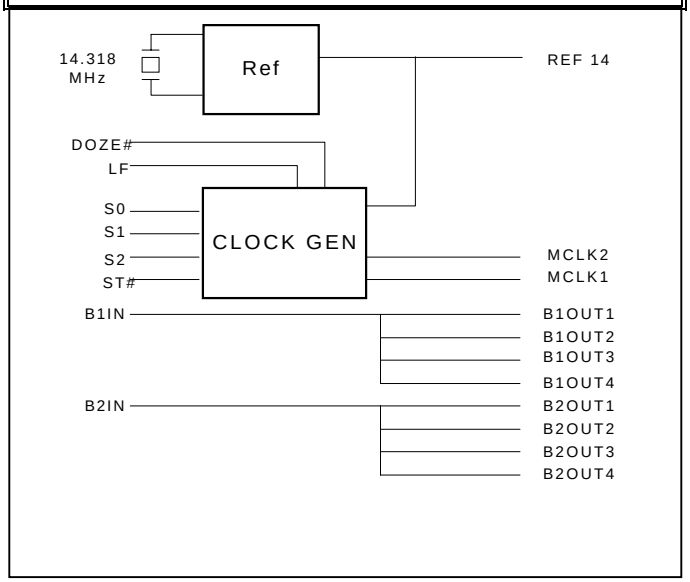
Motherboard Clock Chip

Approved Product

PRODUCT FEATURES

- Generates All Essential Clock signals for the Motherboards
- 3.1V to 5.5V Operating Supply Range
- Supports 8086, 80286, 80386 and 80486 including S Series® and Pentium™ Based Designs
- supports ISA, VESA, and PCI Based Designs
- Supports GREEN PC Applications
- On-chip dual QUAD Buffers with 60 mA Switching Current and CMOS Switching Threshold
- Wide range of selectable output frequencies including 80, 66.6, 60, 50, 40, 33.3, 16 and 8 Mhz
- DOZE mode for low power consumption
- Separate B1 Buffer VDD supports mixed 5V/3.3V outputs
- Smooth and glitch-free switching during DOZE# to be activie
- 50% duty cycle
- TTL or CMOS compatible outputs
- Low, short and long term jitter
- 28 PDIP and 28 PIN SSOP (209 Mil body) package options

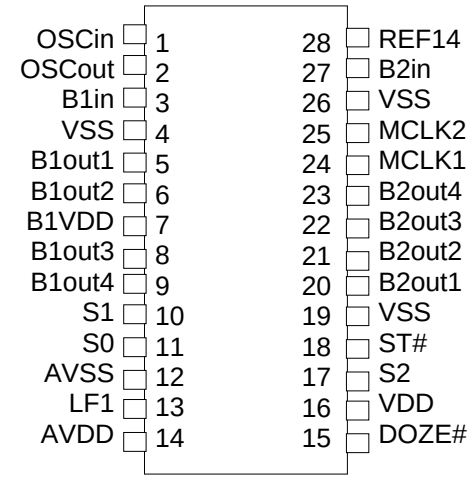
BLOCK DIAGRAM



PRODUCT DESCRIPTION

The IMISc484 is a clock chip for Motherboards. The IMISc484 includes two independent VCO's and uses a single 14.318 Mhz external crystal to generate all essential clock signals. The IMISC484 is designed to generate CPU clock options of 80 MHz, 66.6 MHz, 60 Mhz, 50 Mhz, 40 Mhz, 33.3 Mhz, 16 Mhz and 8 Mhz, giving flexibility to the user. The frequency selection on the MCLK outputs is determined by the S0-S2 pins. In addition, the REF14 output provides a buffered (14.318 Mhz) output. DOZE# pin give additional flexibility to the user for Green PC applications. Activating the DOZE# pin smoothly switches the MCLK output to preprogrammed DOZE frequencies. Deactivating the DOZE input allows the CPU output to return to full speed. On-chip buffers provide the needed buffering for PCI or VESA applications.

P- DIP/SSOP CONNECTION DIAGRAM



APPLICATIONS

IMISC484 eliminates the need for multiple oscillators and generates all the essential clock signals for the Personal Computer Motherboards. Supports 8086, 80286, 80386SX, 80386DX, 80486SX, 80486DX, 80486DX2, 80486 S Series®, and Pentium™ based designs. IMISC484 can be used with Green PC, laptop or notebook computers to save power by running the system slower than normal CPU speeds.

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PIN DESCRIPTION

OSCin, OSCout - These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (nominally 14.318 Mhz). OSCin may also serve as input for an externally generated reference signal.

S0, S1, and S2 - Standard frequency select inputs. These inputs control the high speed MCLK frequency selection. S0-S2 inputs control the CPU clock frequencies. All these inputs have internal pull-ups.

Tables 1 and 2 show the output frequency selection conditions.

MCLK2 - Master clock output. Programmable output frequencies can be selected using S0-S2 inputs shown in Table 1.

DOZE# - DOZE control pin. When DOZE# is high, the clock chip operates in the standard mode. When this pin goes low, output frequencies are switched to the preprogrammed DOZE frequencies. Switching to DOZE frequencies occurs smoothly to allow tracking by 486 CPU internal PLL. This pin has an internal pull-up.

B1in and B2in - On-chip buffer inputs. These pins have internal pull-ups.

B1out1, B1out2, B1out3, and B1out4 - Buffered output pins of B1in. These buffers are capable to sink or source 60 mA switching current. They can be used to buffer critical clock lines for PCI or VESA applications. When these signals are in a high state, they follow the supply applied at B1VDD (Pin 7). If B1VDD is 3 volts, the B1out swings between 0 and 3 volts even if the IC is running at 5 volts.

B2out1, B2out2, B2out3, and B2out4 - Buffered output pins of B2in. these buffers are capable to sink or source 60 mA. they can be used to buffer critical clock lines for PCI or VESA applications.

MCLK1 - Master clock ouput divided by 2 (MCLK2/2).

ST# - Doze frequency select input. This pin controls the frequency of MCLK2 when in the DOZE mode.

REF14 - 14.318 Mhz output. Buffered output of on-chip reference oscillator or externally provided reference.

LF1 - This is the phase detector output for use as loop error signal. A 0.1uF capacitor to ground should be connected from this pin to form the loop filter.

VSS - circuit ground

VDD - Positive power supply.

AVSS - analog circuit ground.

AVDD - Analog positive power supply.

B1VDD - 3.3v/5v logic level control for B1 buffer.

SC484 FREQUENCY TABLE					
INPUTS			MCLK2 (Mhz)		
S2	S1	S0	DOZE# = 1	DOZE# = 0	
				ST=1	ST=-0
0	0	0	66.6	33.3	33.3
0	0	1	80	33.3	33.3
0	1	0	60	33.3	33.3
0	1	1	50	33.3	33.3
1	0	0	33.3	8	16
1	0	1	40	8	16
1	1	0	50	8	16

TABLE 1

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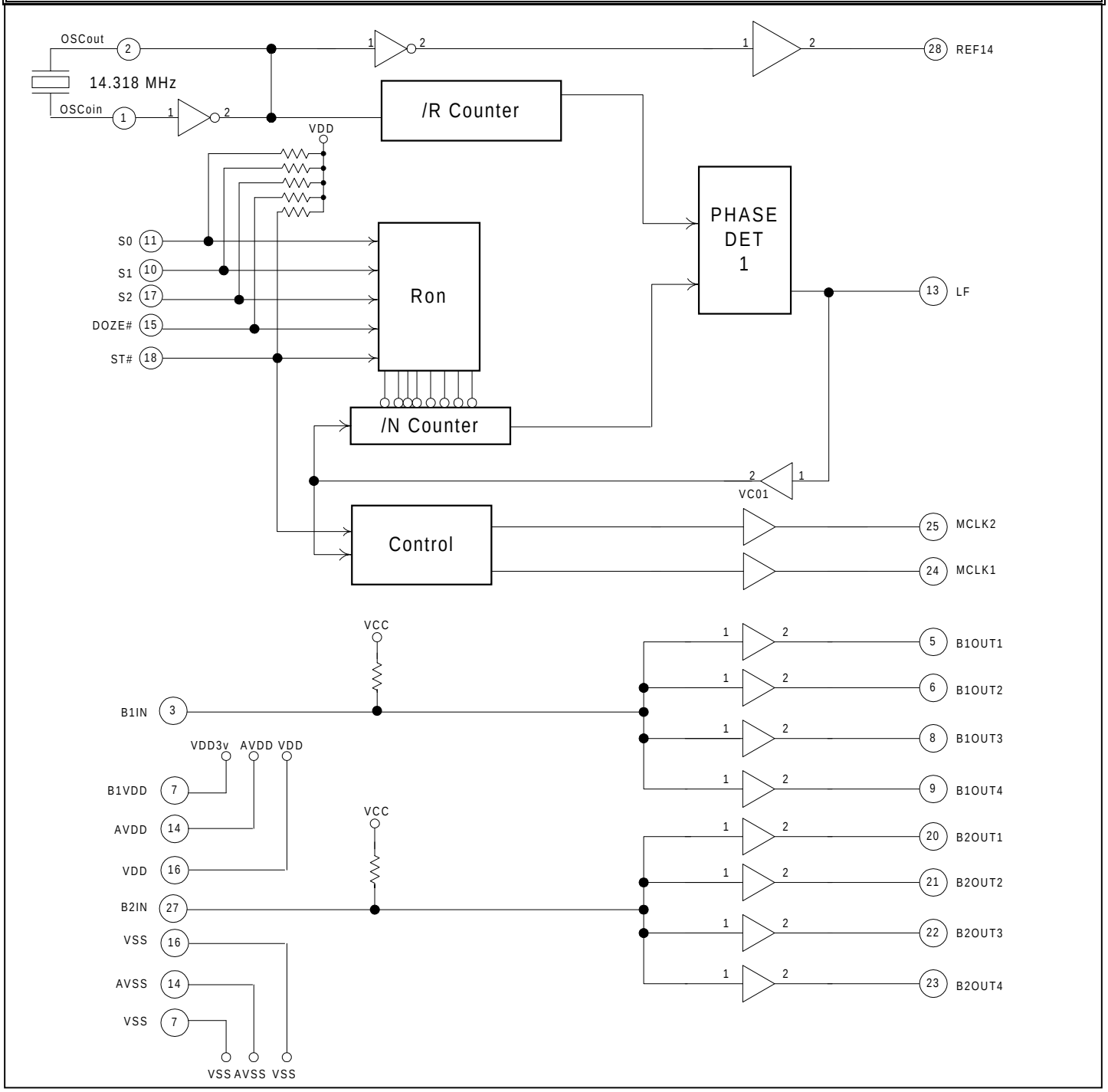
BLOCK DIAGRAM



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MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V to 6V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-65° to + 150°C
Ambient Temperature:	-55°C to + 125°C
Recommended Operating Range:	3V-6V

This device contains circuity to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

$V_{SS} < (Vin \text{ or } Vout) < V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	All Inputs
Input High Voltage	VIH	2.0	-	-	Vdc	All Inputs
Input Low Current	IIL	-	-	5	µA	S0-S2 Inputs
With Pull-up or Pull-down				± 50		
Input High Current	IIH	-	-	5	µA	S0-S2 Inputs
With Pull-up or Pull-down				± 50		
Output Low Voltage IOL = 6 mA	VOL	-	-	0.4	Vdc	All Outputs
Output High Voltage IOH = 6 mA	VOH	2.4	-	-	Vdc	All Outputs
Tri-State Leakage Current	IOZ	-	-	10	µA	LF1, LF2 and LF3
Dynamic Supply Current	ICC	-	-	35	mA	VDD @ 5V, MCLK2 = 50 Mhz
Short Circuit Current	ISC	25	-	-	mA	1 output at a time - 30 sec.

VDD = +3.3 ± 10%, TA = 0°C to + 70°C

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SWTICHING CHARACTERISTICS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Output Rise (0.8V - 2.0V) and Fall (2.0V-0.8V) time All Outputs	tTLH, tTHL	-	-	1.5	ns	15 pf Load
Duty Cycle MCLK and REF14	-	45	50/50	55	%	Measured at 1.4V
Propagation Delay Bin to Bout	tTLH, tTHL	3*	3.6*	6*	ns	15 pf Load Measured at 1.4V
Buffer out Skew B1out1-B1out4 or B2out1-B2out4	tSKEW	-	250	-	ps	15 pf Load Measured at 1.4V
Jitter One Sigma MSLK and REF14	tj1s	-	-	$\pm$ 2	%	As Compared with Clock Period
Jitter Absolute MCLK and REF14	tjab	-	-	$\pm$ 5	%	As Compared with Clock Period
Switching Current Low	IOL(AC)**	-	60*	-	mA	VOL = 1.5V
Switching Current High	IOH(AC)**	-	50*	-	mA	VOL = 1.5V, B1VDD $\geq$ 3.1V
						B1VDD = 3.3 $\pm$ 10%, VDD = AVDD = 5 $\pm$ 10%, TA = 0°C to 70°C

*For VDD = +5V + 10% operation only.

**IOL(AC) and IOH(AC) are reduced by 45% at VDD = 3.3V.

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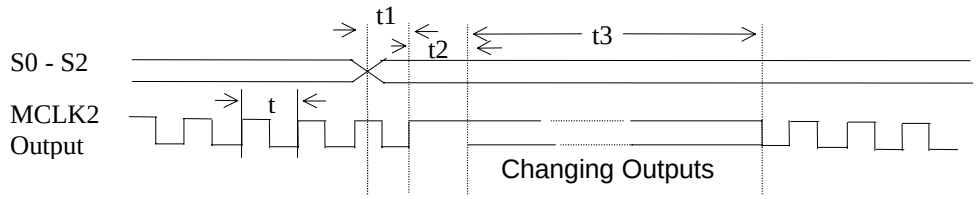
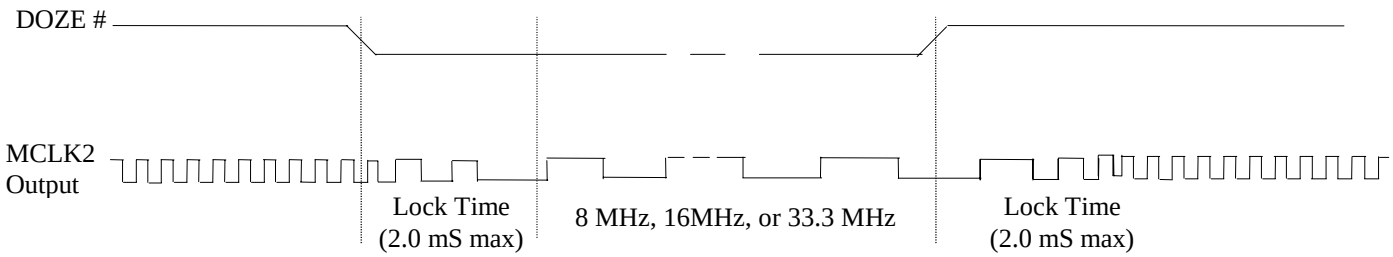
TIMING DIAGRAMS

Standard Mode



t: Current cycle time
t1: Time to first positive edge after address change
t2: Ouput high time. t2 - 4 t
t3: Lock time. 2.0ms max

DOZE Mode
(MCLK2: Switching to 8 MHz, 16 MHz or 33.3 MHz



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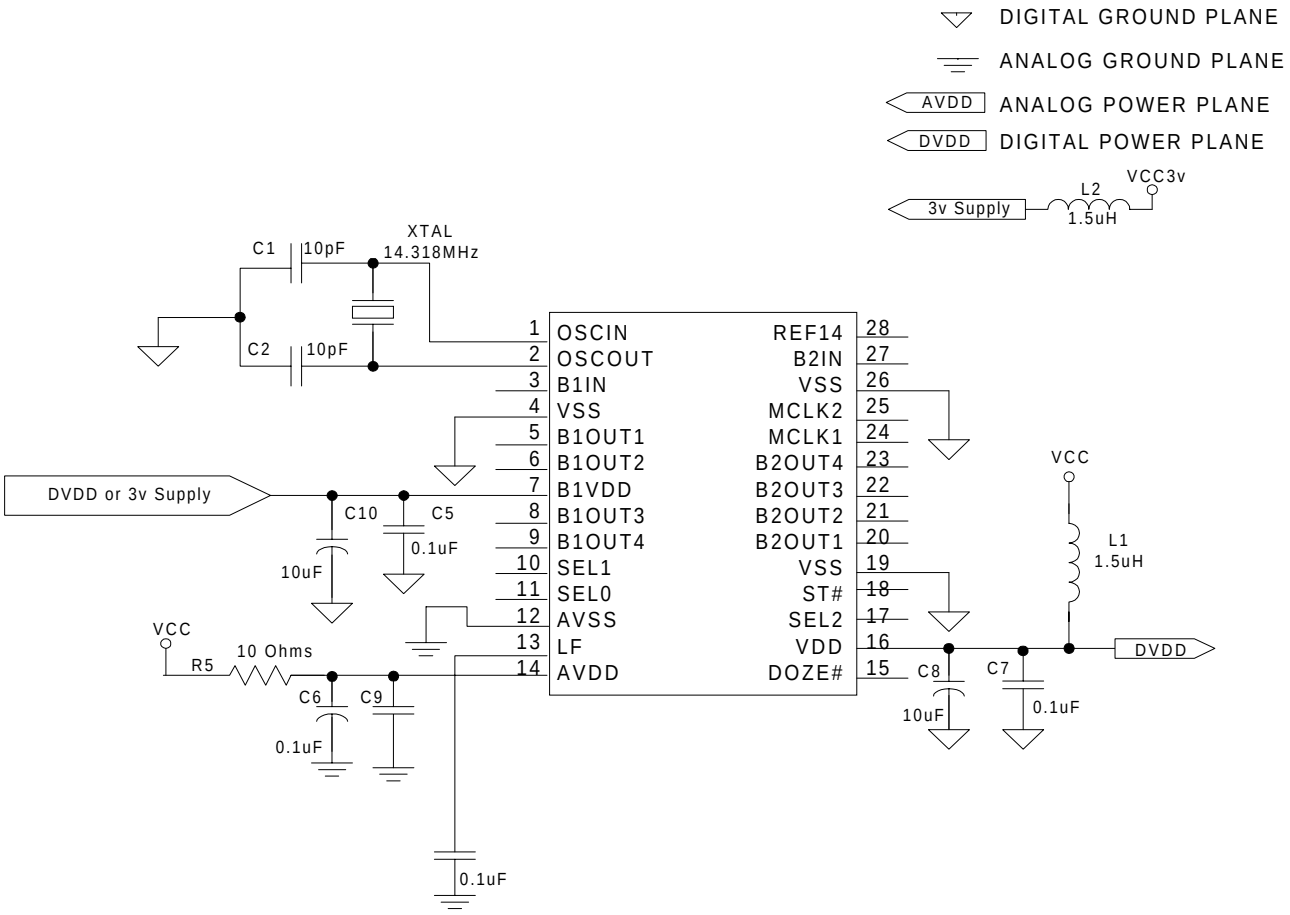
APPLICATION DIAGRAM



NOTE1: C5, C6, C7, C8 C9 AND C10 MUST BE CLOSE TO THEIR VDD PINS

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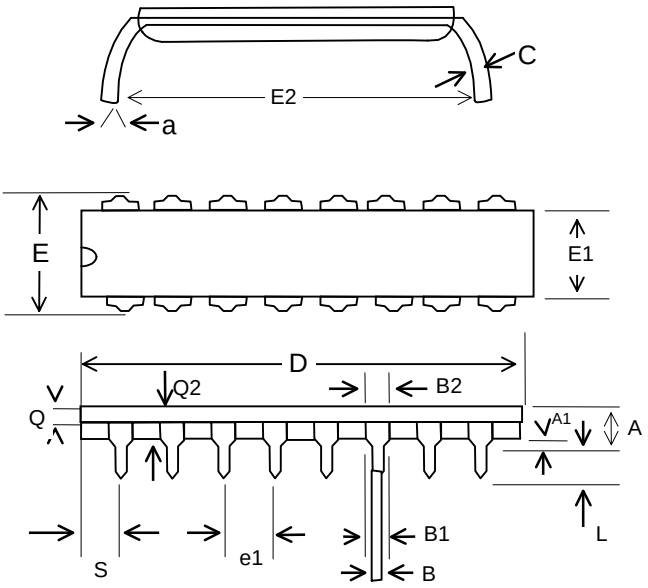
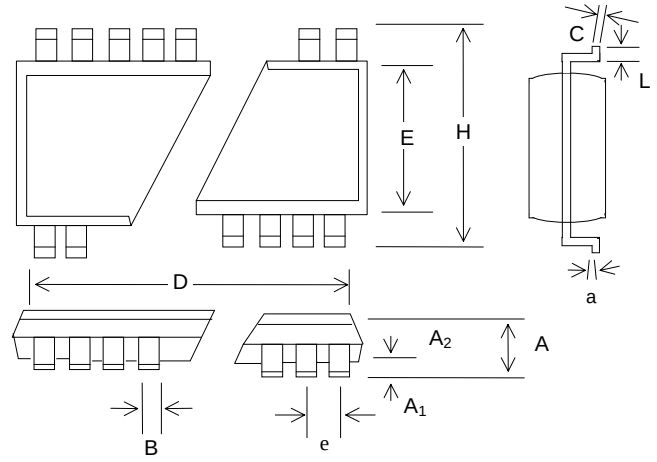
PACKAGE DRAWING AND DIMENSIONS



28 PIN SKINNY PLASTIC DIP DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.180	-	-	4.57
A_1	0.020	-	-	0.51	-	-
B	0.015	0.0.8	0.020	0.38	0.46	0.51
B_1	0.045	0.050	0.055	1.14	1.27	1.40
B_2	0.035	0.040	0.045	0.89	1.02	1.14
C	0.008	0.010	0.012	0.20	0.25	0.30
D	1.360	1.365	1.370	34.54	34.67	34.80
E	0.300	-	0.325	7.62	-	8.255
E_1	0.280	0.282	0.284	7.11	7.16	7.2`
E_2	0.282	0.284	0.286	7.16	7.21	7.25
e_1	0.100 BSC			2.54 BSC		
L	0.128	0.130	0.135	3.18	3.30	3.43
a	0°	7°	15°	0°	7°	15°
Q_1	0.055	0.060	0.065	1.40	1.52	1.65
Q_2	-	130	-	-	3.30	-
S	0.028	0.033	0.038	0.71	0.84	0.97



28 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.08	0.073	0.078	1.73	1.8	1.99
A_1	0.002	0.005	0.008	0.05	0.13	0.21
A2	0.066	0.068	0.070	1.68	1.73	1.78
B	0.010	0.012	0.015	0.25	0.30	0.38
C	0.005	0.006	0.009	0.13	0.15	0.22
D	0.397	0.402	0.407	10.07	10.20	10.33
E	0.205	0.209	0.212	5.20	5.30	5.38
e	0.65 BSC			0.0256 BSC		
H	0.301`	0.307	0.311	7.65	7.80	7.90
a	0°	4°	8°	0°	4°	8°
L	0.022	0.030	0.037	0.55	0.75	0.95

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ORDERING INFORMATION		
Part Number	**Package Type**	**Production Flow**
IMISC484CPB	28-Pin Plastic Dip	Commercial, 0°C to + 70°C
IMISC484CYB	28-Pin SSOP	Commercial, 0°C to + 70°C

Marking Example: IMI
SC484CPB
Date Code
Lot #

IMISC484CPB

Flow

B = Commercial, 0°C to + 70°C

Package

P = Plastic Dip
Y = SSOP

Revision

IMI Device Number